REMARKS/ARGUMENTS

Claims 1-3, 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Owada et al. (5,220,199). Claims 1, 2, 4-11, 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art (AAPA). Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owada et al. in view of Viswanadam et al. (6,759,319). Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owada et al. in view of Ishikawa et al. (JP Patent 2003017530). Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Owada et al.

1. Rejection of claims 1-3, 5-7 under 35 U.S.C. 102(b):

Claims 1-3, 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Owada et al. (5,220,199), for reasons of record that can be found on page 2 in the Office action identified above.

For definitely presenting the characteristics of the present application, the applicants have amended claim 1 as shown in the "Listing of Claims" section. According to the amended claim 1, the claimed object is related to a **dummy** solder bump structure which is not electrically connected to any other elements or devices on the substrate and only functions to improve the fluidity of an underfill liquid compound in subsequent packaging processes. Furthermore, the main characteristics of claim 1 include *there is no metal conductive layers formed between the UBM layer (58) and the dielectric layer (50 or 48) so that the solder bump (60) dose not electrically connect with the conductive layer (46)* (shown in Fig. 9).

However, the solder bump (2) according to the application of Owada et al. is

electrically connective with other elements on the substrate (1), since the electrode pad (6) electrically connects the solder bump (2) to the Al wiring (3), wherein the Al wiring (3) constitutes the power source wiring for supplying the power source to the internal circuits (col.4, lines 58-62). In other words, *the solder bump (2) of Owada et al. serves as an electrical interconnection device for electrically connecting other microelectronic devices on the chip (1), while the structure according to the amended claim 1 of the present application is a* ***dummy solder bump structure*** *having no contribution of electrical interconnection.* Therefore, the solder bump structure of Owada et al. is quite different from the dummy solder bump structure of the present application, and the present application is not anticipated by Owada et al. Reconsideration of the amended claim 1 is hereby requested.

Since claims 2-3, 5-7 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of claims 2-3, 5-7 is politely requested.

2. Rejection of claims 1,2,4-11, 13-17 under 35 U.S.C. 102(b):

Claims 1,2,4-11, 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's admitted prior art (AAPA), for reasons of record that can be found on pages 3, 4 in the Office action identified above.

According to the amended claim 1 of the present application, *under the dummy solder bump, there is no metal pad (56) between the UMB layer (58) and the dielectric layer (48)* since the dielectric layer is completely cover the conductive layer, *while in AAPA, there is a metal pad (24) under every solder bump.* In addition, in the present

application, the passivation layer (50) is preserved between the UMB layer (58) and the conductive layer (46), so as to prevent the formation of the parasitic capacitance that may formed between the metal pad (24) and the conductive layer (16) in AAPA. Therefore, the dummy solder bump of the amended claim 1 of the present application has significant differences from AAPA. (Please refer to Fig 4 and Fig. 9.)

Since claims 2, and 4-9 are dependent upon claim 1, they should be allowed if claim 1 is allowable. Reconsideration of claims 2, and 4-9 is politely requested.

In addition, claim 10 is amended according to Fig.8 and Fig.9 to further emphasize the character of the positions where the via plug and the metal pad are formed. No new matter is introduced. *According to the amended claim 10 of the present application, the via plug (54) and the metal pad (56) are only formed within the first area.* On the contrary, *according to the AAPA, the metal pads (24) are formed both within the first area and the second area.* (Please refer to Fig. 4.) Therefore, there are significant differences between the method of the present application and the AAPA.

As a result, reconsideration of claim 10 is politely requested. Since claims 11 and 13-17 are dependent upon claim 10, they should be allowed if claim 10 is allowed. Reconsideration of claims 11 and 13-17 is politely requested.

3. Rejection of claim 4 under 35 U.S.C. 103(a):

Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owada et al. in view of Viswanadam et al., for reasons of record that can be found on pages 4, 5 in the Office action identified above.

Claim 4 is dependent on claim 1, and thus should be allowed if claim 1 is allowed. Reconsideration of claim 4 is politely requested.

4. Rejection of claim 9 under 35 U.S.C. 103(a):

Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owada et al. in view of Ishikawa et al., for reasons of record that can be found on page 5 in the Office action identified above.

Claim 9 is dependent on claim 1, and thus should be allowed if claim 1 is allowed. Reconsideration of claim 9 is politely requested.

5. Rejection of claims 3, and 12 under 35 U.S.C. 103(a):

Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Owada et al., for reasons of record that can be found on page 5 in the Office action identified above.

Claim 3 is dependent on claim 1 and claim 12 is dependent on claim 10, and thus should be allowed if claim 1 and claim 10 are allowed. Reconsideration of claim 3 and claim 12 is politely requested.

6. Addition of new claim 18:

The solder bump structure of Owada et al. has a contact hole (4) to expose the conductive layer (the Al wiring 3 in Fig.4), so that the conductive layer can electrically

connect the electrode pad and the solder bump. As a result, for clearly describing the difference between Owada et al. and the present application, a new claim 18 is added according to Fig.9 to define the relative position of the dummy solder bump of the present application. As shown in Fig.9, the conductive layer (46) is positioned below the dielectric layer (48) and the passivation layer (50) without contacting the UBM layer (58). No new matters are introduced. Consideration of the new claim 26 is thereby politely requested.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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